ABSTRACT OF THE DISCLOSURE

[1130] An exemplary NAND string memory array provides for capacitive boosting of a half-selected memory cell channel to reduce program disturb effects of the half selected cell. To reduce the effect of leakage current degradation of the boosted level, multiple programming pulses of a shorter duration are employed to limit the time period during which such leakage currents may degrade the voltage within the unselected NAND strings. In addition, multiple series select devices at one or both ends of each NAND string further ensure reduced leakage through such select devices, for both unselected and selected NAND strings. In certain exemplary embodiments, a memory array includes series-connected NAND strings of memory cell transistors having a charge storage dielectric, and includes more than one plane of memory cells formed above a substrate.